PITT STREET RESEARCH

Adisyn Ltd.

Next generation computer chips

Share Price: A$0.07

ASX:AI1

Sector: Technology

14 January 2025

Transistors in computer chips are getting smaller and smaller, but the electrical connections between these transistors are struggling to keep up with this miniaturisation. Today's copper interconnections cannot scale down much further due to the inherent limitations of the metal at very narrow linewidths, i.e. smaller than 5 nanometers. To continue scaling beyond the 2nm node, major breakthroughs in interconnect, contact design and process technologies are needed. Other materials with better electrical characteristics that are faster and produce less heat, are required to connect tomorrow's transistors if Moore's Law of ever-shrinking computer chips is to be followed. Enter 2D Generation.

Interconnects made of graphene to the rescue

Adisyn Ltd. (ASX:AI1) recently acquired Israel-based 2D Generation, which has been researching graphene as a material to connect very small transistors. Graphene has been demonstrated to have a number of very favourable electrical characteristics, even in very narrow linewidths. If it can be used to connect transistors smaller than 2 nanometers, it could be the solution to the hard wall of copper interconnects that the semiconductor industry is running into.

A global growth opportunity

2D Generation has been developing its graphene deposition technology for four years and anticipates it will be able to deliver a demo prototype in 2026. Partial Proof-of-Concept has already been demonstrated. It has been working with world-renowned semiconductor research institute imec and has been accepted into ConnectingChips, a development program that is part of the EU Chips Act that also involves NVDIA, the world's leading supplier of AI chips. If 2D Generation succeeds in delivering a full POC, it will have solved major fundamental material issues in the chip industry and a potential takeover by one of the major semiconductor equipment companies is a distinct possibility.

Strong growth in Adisyn's existing business

Adisyn's existing services business provides managed technology services and solutions, aiming to be the preferred sovereign provider for SMEs in the Australian defence industry supply chain. We think this business represents a growth opportunity too, albeit at a domestic scale.

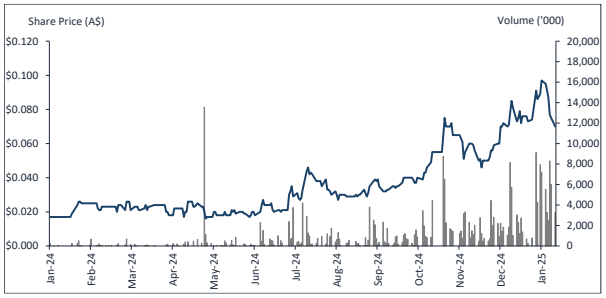
Sum-of-the-Parts valuation of A$0.29 per share

We have valued Adisyn using a Sum-of-the-Parts valuation given that we believe the company's two business are quite distinct and could potentially be operating and/or divested on a standalone basis. We currently value AI1 at A$0.29 per share - $0.22 for 2D and $0.07 for the legacy business. Please see page 26 for the key risks to our thesis.

Market cap. (A$ m)	43.2
# shares outstanding (m)	617.3
# shares fully diluted (m)	994.3
Market cap ful. dil. (A$ m)	69.6
Free float	50%
52-week high/low (A$)	0.10 / 0.016
Avg. 12M daily volume ('1000)	993.9
Website	www.2dgeneration.com www.adisyn.com.au

Source: Company, Pitt Street Research

Share price (A$) and avg. daily volume (k, r.h.s.)



Source: Refinitiv Eikon, Pitt Street Research

Sum-of-the-Parts Valuation	
Valuation 2D Generation (A$)	0.22
Valuation Services business (A$)	0.07
Overall Adisyn valuation (A$)	0.29

Source: Pitt Street Research

Disclosure: Pitt Street Research directors own shares in Adisyn.

Analysts: Marc Kennis, Nick Sundich

Tel: +61 (0)4 3483 8134

marc.kennis@pittstreetresearch.com

nick.sundich@pittstreetresearch.com

Table of Contents

The Adisyn investment case

- Adisyn Ltd (ASX:AI1) recently acquired 100% of the shares of Israel-based 2D Generation that is developing the next generation technology to connect computer transistors. Today's transistor interconnects use copper, but as the transistor design rules become ever smaller, the interconnects need to become smaller as well to deliver the increase in performance. However, copper as an interconnect metal is running into serious physical limitations when the linewidths become very small.
- 2D Generation aims to develop tomorrow's interconnect using graphene, which has a number of key advantages over copper when scaling below 2 nanometers. The company has been working on depositing graphene on semiconductor substrates through a process called Atomic Layer Deposition (ALD) for four years and aims to deliver a Demo Prototype in 2026.
- 2D Generation is working with leading semiconductor research institute imec and several large technology companies, including NVDIA, to drive graphene ALD forward.
- If and when a Demo Prototype is delivered, we believe there will be very serious interest from the semiconductor industry to license or own the technology. We would expect semiconductor equipment companies (OEMs), leading edge chip manufacturers and fabless chip companies alike to be interested in 2D Generation's graphene deposition technology.
- Arye Kohavi, the co-founder and CEO of 2D Generation, has a successful track record in founding several global technology firms and establishments of deep cooperation with some of the world's leading companies. Mr. Kohavi has been chosen as one of the world's top 100 Leading Global Thinkers and one of the world's top innovators.
- Apart from interconnects in semiconductors, the core technology 2D Generation has developed for graphene deposition has many other application areas, including energy storage, Quantum Computing, photonics and optoelectronics. These application areas may potentially be addressed by the company in the future, opening up additional, potential revenue streams.
- Meanwhile, Adisyn's existing services business shows a lot of potential in a world where Australia's defence supply chain will increasingly require a sovereign and secure data center backbone. This business is essentially a domestic, Australian growth opportunity that should reach profitability in the near to medium term.
- On a Sum-of-the Parts basis, we value Adisyn at A$0.29, i.e. A$0.22 for 2D Generation and A$0.07 for the services business. We can see a scenario where either business can be spun out independently, depending on valuations and market demand at that time.
- Specifically for 2D Generation, we believe semiconductor OEMs, such as Applied Materials, Lam Research, ASM International and Tokyo Electron, will be the most likely potential strategic buyers in an M&A scenario.

We see the following share price catalysts:

- We expect 2D Generation will have regular news flow around its graphene deposition development work in the near to medium term.
- Positive progress reports around the company's work with imec and the ConnectingChips collaboration.
- Possible announcements of additional semiconductor industry collaborations in the near to medium term.
- Appointment of top global industry leaders to the company's management.
- Delivery of a Demo Prototype of graphene interconnects using ALD, expected in 2026.
- The services business becoming profitable, expected within the next 18 months.
- Potential takeover/divestment of either Adisyn's existing services business and/or 2D Generation in due course.

Smaller transistors require smaller interconnects … and that is becoming a big problem

When it comes to computer chip manufacturing, smaller is better for a lot of reasons. Smaller chips are faster and more energy efficient for one thing. And you can fit more of them on a semiconductor wafer making them cheaper per unit.

Chip circuitry is getting smaller with every iteration.

Over the last 6 decades, chip size reduction has roughly followed Moore's Law, which says that the number of transistors on a chip will double about every 18 to 24 months with a minimal rise in cost. This implies the resolution of chips (the linewidth of the chip circuitry) needs to shrink substantially as well in every new iteration without a significant rise in manufacturing cost.

Since its inception in the middle of the last century, the semiconductor industry has been very successful in bringing down chip resolutions to the point that today's most advanced chips are mass-manufactured at resolutions of 3 nanometres (nm). Three semiconductor manufacturers are currently preparing for mass production at 2nm and below in 2025, specifically TSMC, Samsung and Intel.

> *To give the reader a sense of scale, a nanometer is one billionth of a meter and the human hair grows about 13 nanometres per second!*

As chips get smaller, certain metals just can't be used anymore.

A lot of innovation and fundamental physics research has gone into chip manufacturing in the last 60 years to enable the industry to currently manufacture at 3nm. However, as chips gets smaller and smaller, certain materials and metals have started to reach the limits of their usefulness, at least in computer chip manufacturing, specifically copper.

What are interconnects?

Copper is widely used in chip manufacturing to connect individual transistors through so-called interconnects. As the name suggests, interconnects form the connections between different elements on a chip. Interconnects come in various sizes with the biggest ones, called global interconnects, sitting at the upper levels of a chip forming connections to the larger elements of a chip. You can think of them as the electric highways of a chip.

Semiconductor interconnects are similar to the road network in a city.

Intermediate interconnects sit in the middle part of a chip forming more granular connections within smaller areas of a chip, like roads in a city. Lastly, local connections to individual transistors are made using local interconnects, similar to how streets in a neighbourhood connect individual houses (see Figure 1).

As transistors and the overall circuitry of chips shrink, or scale, interconnects need to shrink as well, because it doesn't make sense to connect a 3nm transistor with a 20nm local interconnect, for instance. That would negate a lot of the benefits you get from building 3nm transistors in the first place!

Copper Interconnects below 10nm run into serious scaling issues

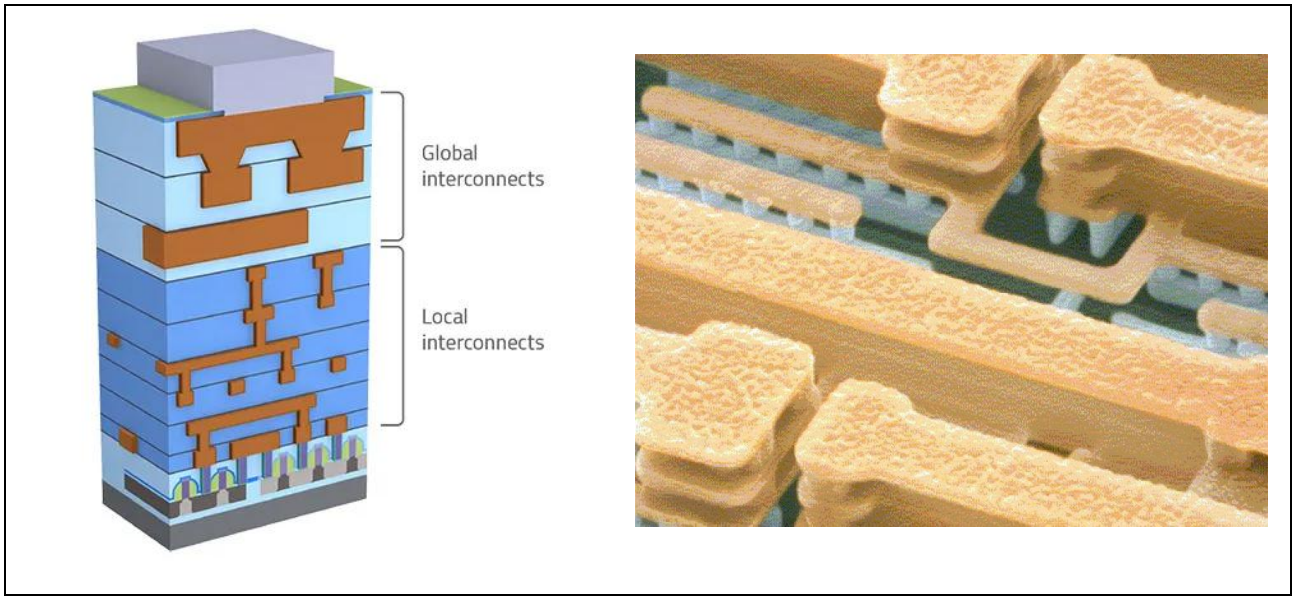
Copper interconnects below 10nm become much less efficient.

However, as copper interconnects get smaller, especially below 10nm, certain problems arise. The most pressing one is that, due to scaling below 10nm, copper's effective resistivity increases very substantially. In turn, this

increases energy consumption of the chip and also increases heat generation, two things you don't want in shrinking semiconductors.

Furthermore, it limits data transfer rates through the copper wires. And as interconnects get smaller, it's easier for electrons to leak out of the interconnect, requiring the use of better barriers, which adds costs to the overall manufacturing process.

Figure 1: Schematic of interconnects (LHS) and copper interconnects as seen through an electron microscope (RHS).



Source: Semiconductor Engineering and IBM

Building smaller copper interconnects is very challenging

Using copper as an interconnect metal below 10nm not only leads to less efficiency and higher manufacturing costs, it is actually very challenging to build this sort of circuitry.

Scaling copper interconnects below 10nm runs into significant manufacturing issues, specifically manufacturing better barriers and liners of the trench that serves as the basis for the interconnect.

Without going into too much detail, most chip circuitry today is built using a process called dual damascene. During this process, the chip circuitry is etched into the substrate using a number of, mostly, chemical process steps.

For interconnects, trenches are created that are subsequently filled with copper. The copper lines need to have proper barriers to prevent current leakage out the sides of the trench. They also need to be capped off once the trench is filled with copper to prevent interaction with the layer that will be built on top.

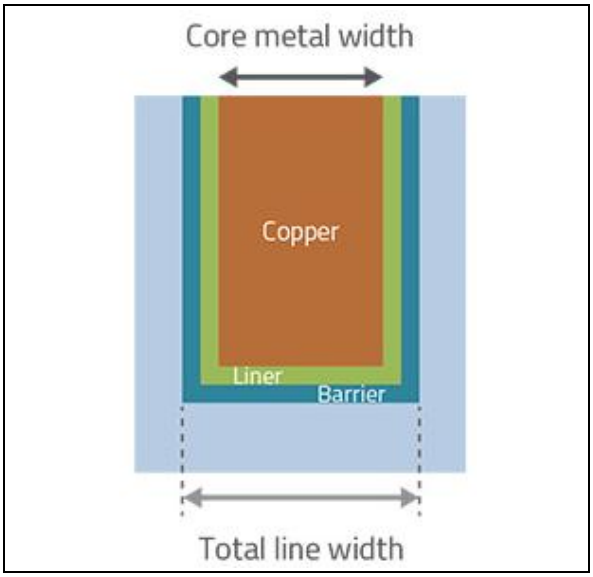
At smaller resolutions, diffusion barriers and liners start to take up too much space.

So-called diffusion barriers prevent copper leakage to adjacent interconnects. Additionally, copper electromigration, the phenomenon of material degradation due to heat build-up, can be mitigated by using adhesion liners between the barrier and the copper. Adhesion liners are also used to form an additional barrier between the copper interconnect and the layer above.

The problem is that the combined width of the barrier and liner, i.e. the wall of the interconnect, cannot be smaller than 2nm to 3nm without compromising effectiveness. So, if a manufacturer wants to reduce the

resolution of the interconnect to, say, 3nm, about 50% of the trench is already taken up by "the wall", leaving not enough space for a sufficient amount of copper to be functional, i.e. sufficient conductivity (see Figure 2). It is important to note that graphene is also defined as a diffusion barrier, and one of 2D Generation's applications is to add graphene to copper, which triples its conductivity.

Figure 2: Copper interconnect with liner and barrier



Source: Lam Research

Multiple solutions are being researched

New materials are being researched.

The semiconductor industry is researching various solutions to the copper interconnect problem, including the use of different metals and alloys that allow for smaller interconnect resolutions without negating the benefits of smaller transistors, i.e. resolutions of 3nm and below. Materials of interest include molybdenum, iridium, cobalt, nickel, rhodium and ruthenium with the latter seemingly being the most promising at the moment.

However, graphene is more than 10 times more conductive than ruthenium and the other proposed solutions. In addition, some of these metals require a different trench manufacturing process, requiring double exposure to Extreme Ultraviolet (EUV) lithography. Explaining EUV goes beyond the scope of this report, but suffice it to say, it is very expensive to begin with and a second EUV process step makes it even more expensive.

But new methods are expensive and require a change in process.

Another, partial, solution to the copper interconnect issue at <10nm resolution is being developed by Intel. So-called backside power delivery moves part of the circuitry to the back of the substrate, i.e. not on the actual chip. This allows for wider circuitry to the transistors on the back of the chip, while creating more space on the chip for other circuitry. But again, this method requires a change in the chip manufacturing process. And if there's anything semiconductor manufacturers don't like, it's changing the way they work because it brings new risks to their processes.

So, what if there was a material that has a lot of advantages without the downsides of the other material being research, and that doesn't require a new way of working on the part of chip manufacturers?

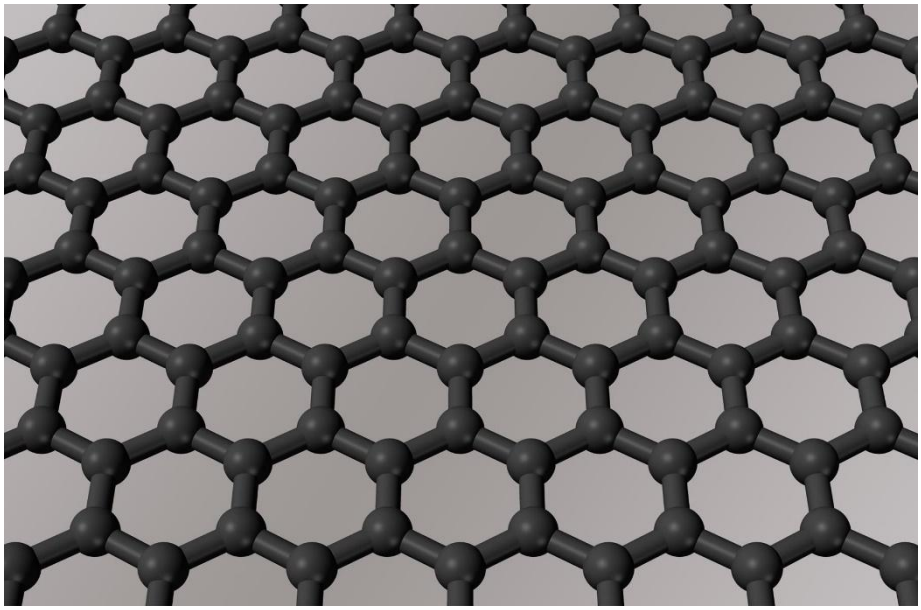
Enter 2D Generation.

2D Generation aims to solve the interconnect problem using graphene

Graphene is a layer of carbon atoms just 1 atom thick.

One of the materials of interest to solve the interconnect resolution issues of copper below 10nm is graphene. Graphene is a layer of carbon atoms just one atom thick, arranged in a hexagonal lattice, or honeycomb structure (Figure 3). Although several large semiconductor equipment companies are researching graphene as a solution to the interconnect problem, we believe 2D Generation is currently working on the most viable option for reasons we will explain below.

Figure 3: The hexagonal shape of graphene



Source: Jynto/Wikimedia Commons

How you build a graphene layer in a semiconductor

Graphene is a remarkable material that delivered its discoverers, Geim and Novoselov, the Nobel Prize in 2010. It's got great electrical conductivity, specifically, it's got high intrinsic carrier mobility and a large current carrying capacity. Graphene also has high thermal conductivity and is 200x stronger than steel.

There are currently four ways to manufacture graphene and graphene layers, only two of which we'll discuss here because they are the only two with relevance to semiconductor manufacturing.

Epitaxial growth of graphene layers in Silicon Carbide semiconductors.

Firstly, epitaxial growth, i.e. the growth of crystalline structures on top of each other, is being applied to grow graphene layers on Silicon Carbide (SiC) wafers to manufacture high-end electronics chips, used in power inverters, electric vehicles etc. However, this is not the area that 2D Generation is focussed on.

Chemical Vapour Deposition is a well-known process.

Secondly, in Chemical Vapour Deposition (CVD), precursor gasses, or reactants, such as methane, hexane, ethanol etc, are pumped into a reaction chamber and heated to very high temperatures (~1,000 C) to make them react with the substrate. In turn, this creates graphene layers on that substrate. Obviously, this is a very simplified description of the process, but you get the drift.

Chemical Vapour Deposition is not up to the task

For decades, CVD has been a widely used method in the semiconductor industry to grow layers on silicon substrates. It's no wonder, then, that the industry first looked to CVD for deposition of graphene layers. In fact, all established semiconductor equipment manufacturers that are currently researching graphene deposition are using CVD, Plasma Enhanced CVD (PECVD) to be precise.

CVD just doesn't cut it anymore when it comes to building increasingly smaller chips.

However, CVD requires operating temperatures of around 1,000 degrees Celsius, which is very high and will damage the chip elements and layers that have been built in previous process steps.

Additionally, even though CVD has been the deposition workhorse for the chip industry for decades, it is less suitable for building integrated circuits (IC's) with smaller resolutions, i.e. below 10nm. As chips get smaller and smaller, more control over layer thickness is required, which CVD increasingly struggles to provide. Which is why the industry started using Atomic Layer Deposition (ALD) for advanced, i.e. smaller resolution semiconductors. ALD is a sub class of CVD.

Depositing graphene using Atomic Layer Deposition

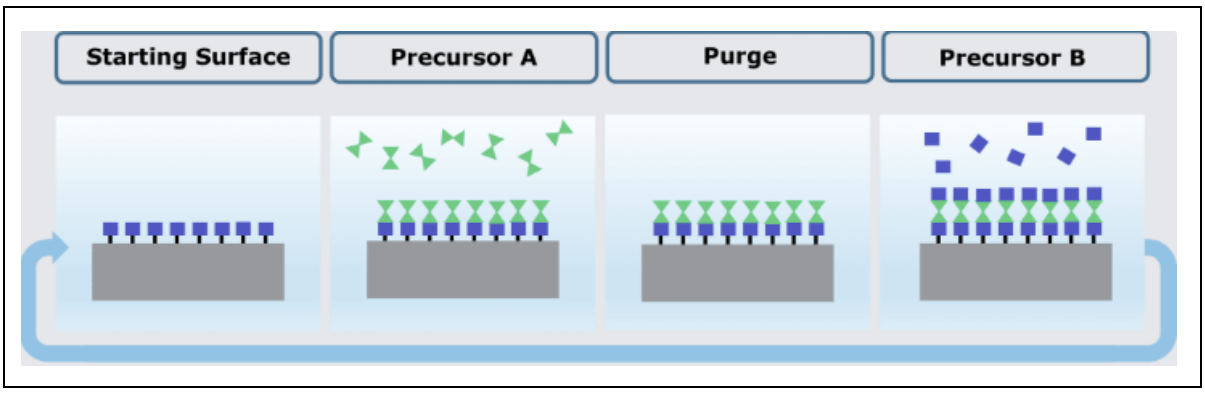
2D Generation is pioneering graphene deposition using ALD.

In order to deposit a single layer of any type of material, Atomic Layer Deposition has become the go-to method of deposition for advanced semiconductor manufacturing in the last ten to fifteen years. But using ALD for graphene deposition to create individual, functional layers in semiconductors has never been done before. In other words, 2D Generation is pioneering this field!

So, what is ALD? In simple terms, Atomic Layer Deposition enables a chip manufacturer to build a very thin film, or layer, on a specific surface. The reason such a film can be extremely thin, i.e. 1 atom thick, is because the two reactant gasses that are used in the process enter the reaction chamber one at a time as opposed to simultaneously, like with CVD.

This means that the reactions in the chamber stop by themselves once all so-called surface sites that a precursor can react with have been occupied. Any leftover precursor will literally just "hang around". Once the reaction has stopped, the chamber is cleared (purged) of any leftover precursor gas and the second precursor is pumped in. Again, the reaction will stop by itself in the same manner (Figure 4). The result is a very thin, uniform layer.

Figure 4: The Atomic Layer Deposition process



Source: Jynto/Wikimedia Commons

The benefits of ALD in chip manufacturing are plentiful:

1) ALD creates very uniform layers, which is good for chip performance.
2) The process provides very precise control of film thickness, down to the atomic level.
3) Many different materials can be used in an ALD process.
4) The process is very well-understood by the industry and is easily scalable and repeatable.
5) Film structures can be easily tuned and engineered depending on the application needed.
6) And last, but certainly not least, ALD can be done at temperatures that are much lower than temperatures used in CVD.

2D Generation's secret sauce

The main advantages of 2D Generation's technology are:

1. Low-temperature process – below 350°C.
2. Growing graphene over non-metal or metal.
3. Capability of selective coverage of graphene, using photolithography.

Low temperature ALD is one of 2D Generation's key advantages.

We are not aware of any other technology in the world that can demonstrate even one of those three advantages individually. And 2D Generation is taking full advantage of ALD's low processing temperature inside the reaction chamber. Typically, process temperatures in 2D Generation's process are below 350 degrees Celsius. This is much lower than ~1,000 degrees required in CVD and has a number of very important benefits:

- **No dopant and layer diffusion:** High processing temperatures can cause different layers and barriers to mix. Also, dopants, which are impurities that have been intentionally introduced to certain materials to improve their performance, can leak away under excess heat.
- **Better material compatibility:** Many modern materials degrade or react poorly at high temperatures, limiting integration options.
- **Less thermal stress**: High temperatures can cause cracking, warping or so-called delamination where one material comes loose from materials below, due to different thermal expansion characteristics between materials.
- **Fewer limitations on deposition tools:** High temperatures accelerate tool wear, increase contamination risks and complicate process control.

Using low-temperature ALD deposition processes, sometimes combined with post-deposition annealing[1], chip manufacturers are able to manufacture high-quality films and layers without risking damage to the underlying layers or substrates, which improves overall yield, i.e. the number of total good (functioning) IC's on a wafer. And maximising yield is the ultimate goal in chip manufacturing, because that is the key driver of a fabrication facility's (fab) profitability.

[1] Heating a wafer and letting it cool down to reduce impurities, improve crystal quality and relieve internal stresses between layers.

Creating proprietary, novel organic precursors

Low temperature ALD is made possible by proprietary graphene molecular precursors.

The main reason 2D Generation is able to create graphene layers at these much lower temperatures is because the precursors used in the process have been specifically chosen to react at lower temperatures.

So, once they enter the reaction chamber, 2D Generation's method doesn't require a process temperature of ~1,000 degrees Celsius to get the reactions started. A temperature below 350 degrees Celsius is sufficient for this, which means this manufacturing process for graphene interconnects below 10nm can take full advantage of the benefits of low-temperature ALD mentioned above.

> *The so-called **graphene molecular precursors** are a compound or a mixture of compounds that, after reaction in the reaction chamber, become part of a graphene coating, film or layer. These novel precursors are part of 2D Generation's Intellectual Property (IP).*

Working with dozens of materials to create optimal precursors.

2D Generation is working with dozens of families of molecules as well as off-the-shelf materials that can potentially serve as precursors that can become graphene and attach to the relevant surfaces. All of these materials are potentially patentable, providing a certain level of IP protection for 2D Generation.

2D Generation owns all the relevant IP rights

So far, the company and the inventor of the initial technology, Professor Doron Naveh of Bar-Ilan University in Israel, has applied for 9 patents around these proprietary precursors and their deposition methods. Eight of those patents are pending while one is in the National Phase (see Appendix III).

Professor Naveh was 2D Generation's Chief Technology Officer (CTO) until September 2022, after which time Paul Rich became the company's Technology Leader. Mr. Naveh has since then transferred all his IP rights, titles and interests, including patents, to 2D Generation and is now a minor shareholder in the company.

Full control over the IP.

Bar-Ilan University, that employs Professor Naveh, transferred all economic rights to the company. Additionally, 2D Generation holds an exclusive commercial license to further develop the IP in this defined field of graphene-based technology. In return, the university had a 10% ownership of 2D Generation and will receive between 1% and 1.5% of future revenues as royalties.

Currently optimising the process recipe

2D Generation was founded in 2020 and has mainly been focussed on optimising the process recipe, i.e. finding out which precursors deliver the best results for certain end goals and applications. That involves preparation of the precursors, introduction of the precursors into the reaction chamber etc. The key parameters in a deposition recipe are:

- Which raw material/precursor to use,
- What temperature the precursor should be prepared at and what temperature the reaction chamber should have,

- Which co-reactant to use,
- What pressure the reaction chamber should be at for optimal reactions,
- What the best timing is for pumping the gasses into the chamber, for the actual reactions/deposition and for the purging of the reactor,
- Which pre-treatment steps to prepare the surface for deposition are needed, and
- What post-treatment steps are needed to enhance the deposited film.

R&D is focussed on building out the IP portfolio by finding the optimal recipes for different precursors.

Testing out a particular recipe and optimising the process in a Design Of Experiment (DOE) approach can take many months. And given the dozens of different materials that 2D Generation is working with, it comes as no surprise that the company's Research & Development (R&D) efforts have been focussed on figuring out the best process recipes for deposition of graphene films, coatings and layers using a variety of precursors with the aim to patent as many different recipes as possible.

Working with semiconductor research powerhouse imec

2D Generation's R&D work has been done in collaboration with imec, the R&D powerhouse located in Leuven, Belgium. imec is one of the world's largest semiconductor R&D facilities and works with all of the industry's bellwethers, including semiconductor manufacturers, semiconductor manufacturing equipment producers and fabless chip companies. As such, imec has extremely good insights into future manufacturing needs and trends as well as the technologies that will be required to make them a reality.

imec very keen to work on 2D Generation's approach to graphene deposition.

And even though all of the incumbent CVD and ALD equipment manufacturers are working on graphene deposition, some in collaboration with imec, it is our understanding that imec has been very keen to work with 2D Generation on its approach to graphene deposition using ALD. Specifically because the company is using ALD rather than CVD, which facilitates low temperature deposition made possible through the use of proprietary precursors.

imec wafers processed in-house

In the current R&D workflow, imec send semiconductor wafers to 2D Generation that have been prepared to the point where the graphene deposition steps can take place. The company dices these wafers into individual IC's (also known as dies) before they are processed in a reaction chamber in multiple batches. Incidentally, in high-volume production environments, the wafers are not diced up into individual IC's until all the so-called front end production is completed and the chips are ready to be packaged.

Once graphene deposition has been completed, the individual dies are analysed by 2D Generation and imec to see how the deposition recipes have worked out and which tweaks need to be made to the recipe to improve the process. The work with imec extends to graphene coating of metal and non-metal materials as well as to various use cases, like surfaces, diffusion barriers and structured wafers.

As mentioned earlier, 2D Generation is performing this work using many different precursors and compounds. Add to that all the temperate, pressure and timing variations in a process recipe, and it's easy to see the amount of R&D work that has gone in to this in the last 4 years.

Current limitations in R&D work

Current processing temperatures are too low.

In this R&D work, 2D Generation is currently facing a number of specific limitations. One of these is the low processing temperature of the reaction chamber the company is currently working with. This current system can only heat up to 180 degrees, which limits the quality of the reactions inside the chamber. For this reason, 2D Generation recently acquired an ALD system from Beneq, based in Finland (Figure 5), which is expected to be delivered in 2Q25.

Figure 5: Indicative Beneq ALD system (Beneq Prodigy)

Source: Beneq

Beneq has a very elaborate background in ALD, having been founded by former design engineers from ASM Microchemistry, part of Netherlands-based ASM International (ASMi), not to be confused with lithography behemoth ASM Lithography (ASML), also from The Netherlands.

ASMi is one of today's CVD and ALD incumbents, and acquired Microchemistry in 1999, which gave it a massive head start in ALD equipment manufacturing well-ahead of the big ALD boom that started in the late 2000's.

So, one could say Beneq is ALD royalty and its equipment is first grade. The tool that 2D Generation has ordered will allow processing up to 500 degrees, i.e. more than enough for 2G Generation's optimal process temperature of up to 350 degrees.

Issue #2: Dealing with contaminated surfaces

The surfaces being processed are not smooth enough pre-ALD processing.

The new Beneq ALD tool can pre clean substrates in situ. This should help alleviate a second issue 2D Generation has been dealing with, i.e. contaminated surfaces of the IC's it's processing.

Hydrogen cleaning smoothens the surface of the IC's prior to processing.

Reacting to outside influences, like oxygen atoms, causes serious defects. In order to counter this effect, 2D Generation has invested in a hydrogen cleaning process that will remove oxides prior to deposition. This improves the interface quality between the graphene and the surface below.

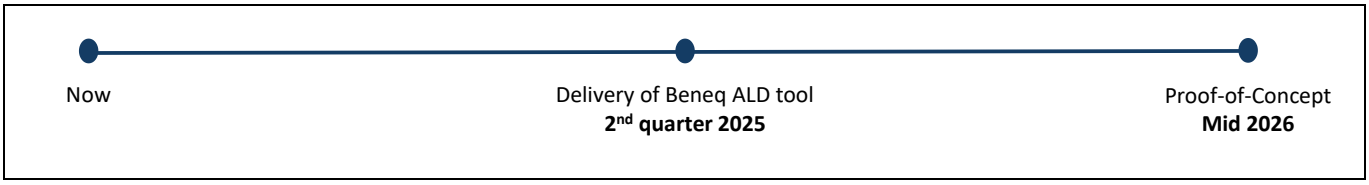
The new Beneq tool facilitates in situ hydrogen plasma, which enables the surface to be cleaned and then deposited without the need to expose the surface to the atmosphere, thereby re-contaminating it. This should substantially improve the company's R&D outcomes once it can start using the tool post-delivery.

Development roadmap towards Demo Prototype

With the Beneq ALD tool slated to be delivered in 2Q25, we expect 2D Generation will be able to substantially step up the speed of its R&D work. Not only will the company be able to speed up processing quite a lot, but it should also achieve much better research outcomes by using a state-of-the-art ALD system with each iteration given the integrated IC hydrogen cleaning process.

2D Generation aims to have a Demo Prototype ready by mid-2026, i.e. proof that its technology is working, on a 1x1cm chip (Figure 6).

Figure 6: Indicative R&D roadmap



Source: Company

Demo Prototype criteria.

The Demo Prototype should demonstrate that graphene interconnects can deliver the following characteristics:

- Graphene interconnects should **reduce signal delay** that is seen with copper interconnects;
- They should lead to **lower power consumption**, which in turn leads to,
- A **better heat profile**, i.e. less heat generation and better heat dissipation, which improves device performance and its lifespan;
- Graphene interconnects need to facilitate **higher density of components** on an individual chip, such as transistors.
- Graphene interconnects should lead to **less crosstalk** between interconnections, i.e. less signal interference, which should result in higher, error-free data transfer rates.

2D Generation is already collaborating in the EU's ConnectingChips initiative.

Once full Demo Prototype has been delivered, 2D Generation will seek collaborations in smaller projects to find application areas for its technology other than graphene interconnects. However, the company is currently already working with ConnectingChips, an initiative by the European Union (EU) aimed at driving innovation and collaboration in the semiconductor industry to make sure the EU stays at the forefront of the semiconductor industry. The company has already received grants for some of this work with more expected. In addition, 2D Generation may receive fees for non-recurring engineering work as part of this project.

Early design inroads through ConnectingChips collaboration

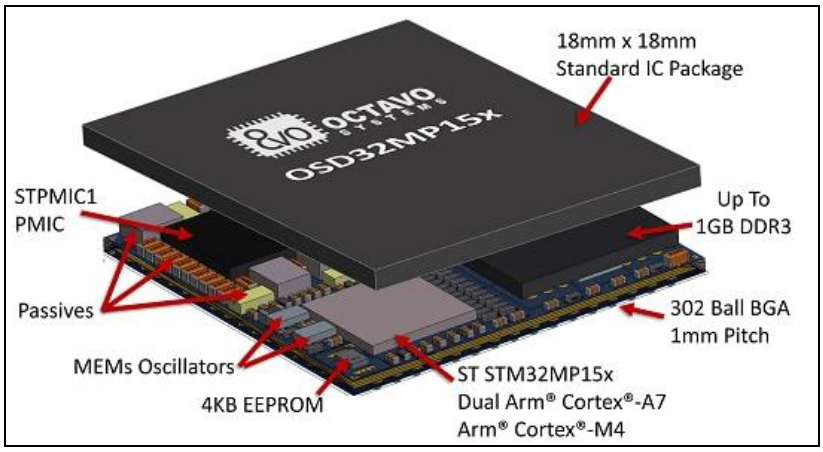
Creating high-performance, next generation chips for AI and autonomous vehicles.

ConnectingChips is a project under the EU's broader Chips Joint Undertaking (Chips JU) initiative, which aims to drive technology research, development and manufacturing capabilities across Europe.

Chips JU runs many high-tech projects simultaneously and the ConnectingChips project will kick off early in 2025. The aim of this project is to establish the next generation of Artificial Intelligence (AI) computing and autonomous vehicles infrastructure based on System-in-a-Package (SiP) development.

That will require development of power efficient high performance electronic, photonic, power and RF chips and System-on-Chips (SoC) as well as their integration into SiP modules. In other words, multiple fully functional compute systems on a single chip get integrated into a larger, but single system in a package (Figure 7). Key benefits of SiP's include smaller footprint, higher energy efficiency with better performance, i.e. processing speed.

Figure 7: System-in-a-Package



Source: STMicro

Once you're in, you're in

Inclusion of the technology in the development phase typically means inclusion of the tech in the final design.

ConnectingChips combines the resources of more than 60 companies and research institutes, including chip manufacturers, chip equipment manufacturers and fabless chip companies. 2D Generation will mostly be collaborating with fabless chip company NVIDIA, Automotive parts supplier Valeo, research institute Fraunhofer and PCB and substrate supplier AT&S.

The beauty of this collaboration is that it allows 2D Generation to be involved in the development and design of next generation IC's for AI and autonomous vehicles from the early onset. If and when these chips subsequently get manufactured in due course, 2D Generation's interconnect technology will most likely be part of the final chip design. It is very rare that technologies get swapped out at the end of these design cycles (if that is even possible). In turn, the inclusion into the final designs will lead to revenues from license fees and royalties. Additionally, it will provide a lot of credibility to 2D Generation as a company and its technology, potentially leading to business from new customers.

We believe the ConnectingChips collaboration is of high strategic importance for 2D Generation and has the potential to cement the company's IP into next-generation semiconductor technology early on.

Other markets 2D Generation could address

Although high end semiconductors, i.e. with resolutions below 3nm, will be the most important application area for 2D Generation's technology, we see others that could be addressed down the track. These include:

- **Energy Storage**: Graphene's high surface area and exceptional electrical conductivity make it a viable material for energy storage applications, like batteries and supercapacitors. Additionally, it can enhance the efficiency of solar cells and improve the thermal management of electronic devices by facilitating heat dissipation.

  Energy storage will be increasingly important as the world moves towards renewable energies that have more intermittent availability than fossil fuels. By minimising heat loss and better power delivery, graphene could help storage devices become more energy-dense and efficient.

- **Biomedicine**: Graphene could be used in biomedical engineering applications, such as drug delivery, biosensors and tissue engineering, specifically as one of the nanomaterials used, because graphene is biocompatible and can be easily functionalised to target specific cells or tissues. They support the absorption and binding of antibodies, adapters, drugs, genes, enzymes and other molecules. Examples of specific applications where graphene may be useful include detection of protein biomarkers and the development of medical scaffolds[2].

- **Coating**: Graphene-based coatings have shown excellent properties, including high mechanical strength, flexibility and corrosion resistance, making them attractive for various industrial applications. In other words, coatings or paints with graphene in them could make the end applications stronger, preventing rust and deterioration. Most obviously such coatings could help transportation devices (such as ships and cars) and can be applied to brick and stone used in houses. But it could even go into food packaging to stop the transfer of water and oxygen molecules, which can cause food quality to deteriorate.

- **Quantum computing**: Graphene's unique electronic properties and compatibility with superconducting materials make it a promising candidate for developing quantum bits (qubits) in quantum computing systems. As we outlined in our research reports on Archer Materials (ASX:AXE), quantum computing is at least 5-7 years away from being commercialised and there are difficulties to be overcome, including the inability of today's technologies to operate at room temperature and the fact that most physical devices are large and difficult to scale.

  Nonetheless, companies and researchers are developing quantum devices and graphene could play a part in it. Graphene has potential to act as a better conductor than silicon, enabling electrons to move with less resistance through the material.

  Researchers in the US found that graphene contains electrons with quantum mechanical, wave-like properties that can be accessed in devices, particularly at very low temperatures[3].

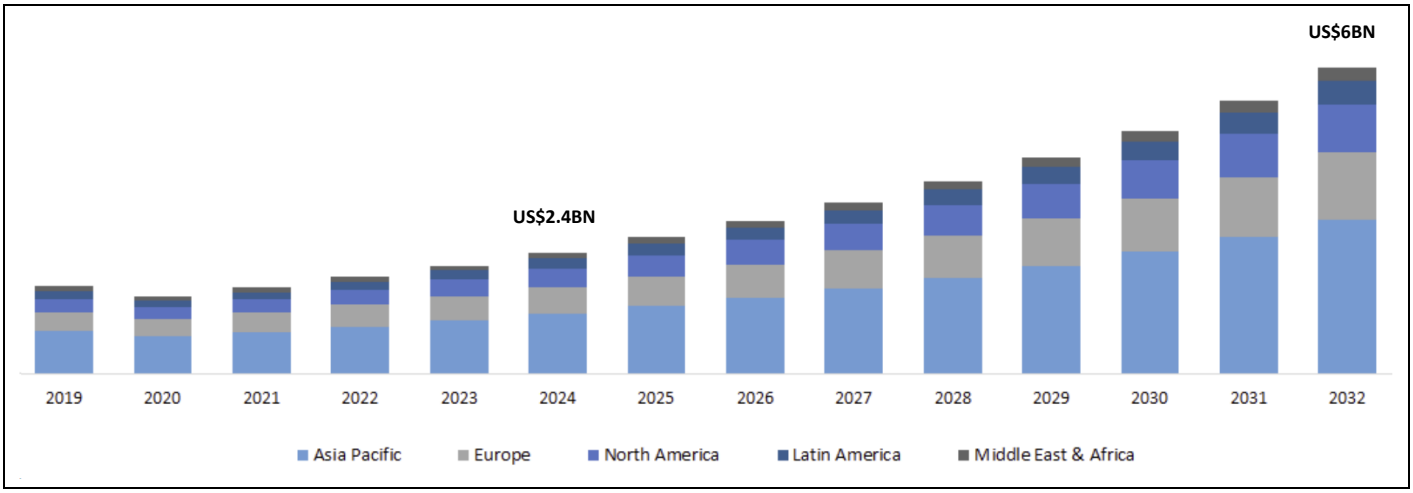
However, despite the many alternative application areas, graphene interconnects is where 2D Generation's full focus is on in the medium term.

[2] https://pmc.ncbi.nlm.nih.gov/articles/PMC6614642/
[3] https://www.livescience.com/technology/electronics/worlds-first-graphene-semiconductor-could-power-future-quantum-computers

The market opportunity for graphene interconnects

As illustrated in the previous chapters, graphene ALD has a number of application areas, the most notable of which is ALD for graphene interconnects. 2D Generation's overall ALD equipment target market is expected to almost triple between 2024 and 2032, from US$2.4BN to just over US$6BN (Figure 8). This includes ALD equipment for the manufacturing of semiconductors, solar devices, medical equipment etc.

Figure 8: Atomic Layer Deposition market size (US$ BN)



Source: Polaris Market Research

To be clear, 2D Generation aims to address the semiconductor subsegment of this overall market and will likely just provide IP around graphene deposition technology, not the deposition hardware.

> *In other words, the company aims to license out its graphene deposition "cookbook" and "recipes" to future customers, not the required "pots, pans and ovens". Those need to be purchased from the semiconductor equipment OEMs.*

Semiconductor equipment companies are the obvious prospects

The most likely customers for 2D Generation's IP are semiconductor equipment companies, or OEMs (Original Equipment Manufacturer), like Applied Materials, ASM International, Tokyo Electron and Lam Research, that currently already sell ALD equipment to chip manufacturers, such as Intel, TSMC, Texas Instruments, NXP, STMicro, GlobalFoundries etc.

Semiconductor OEMs could be interested in licensing or acquiring 2D Generation's IP.

Many of the OEMs are working on graphene deposition technology, but they're all using Plasma Enhanced CVD (PECVD), not ALD. So, they are all working with higher deposition temperatures than 2D Generation does in its ALD process, which means they're having to deal with the drawbacks of this higher-temperature deposition technique.

For this reason, we believe they could, or should, be interested in (exclusively) licensing or acquiring 2D Generation's IP.

Leading edge chip manufacturers will be interested too

The whole purpose of having graphene interconnects is to be able to connect transistors that are smaller than 5nm in order to capture the benefits of these smaller transistors. Connecting transistors that are 7nm and bigger in size can still be done with copper interconnects without losing the benefits of this transistor size (compared to larger transistors, e.g. 10nm). The drawbacks of copper interconnects become much more of an issue at 5nm and especially at 3nm and below.

If you can afford EUV tools, you will need graphene interconnects

However, in order to manufacture transistors of 3nm in size, a chip manufacturer will need very advanced chip equipment, including so-called Extreme Ultraviolet (EUV) lithography systems. In simple terms, lithography is used to transfer the design of a chip onto the wafer, layer by layer.

There is only one company in the world that manufactures EUV systems, which is ASML in The Netherlands. The latest iteration of its system, EUV High-NA (Numerical Aperture), costs upwards of US$350m per unit.

Only the largest chip companies can afford EUV systems and hence produce at 3nm and below.

In other words, only the largest chip manufacturers in the world are able to afford these systems, including TSMC, Samsung, SK Hynix, Intel and Micron. TSMC and Samsung, for instance, are currently using EUV to manufacture critical layers at 3nm and are planning to start volume production at 2nm in 2025 using EUV High NA. Intel aims to start volume production at 1.8nm (18 angstrom) using EUV High NA in 2025.

It is at these very small resolutions where graphene interconnects will shine. Hence, buyers of EUV tools will be very interested in graphene ALD and absolutely need graphene interconnects to get the best performance out of their future chips.

In due time, graphene could be used in less critical resolutions

The successful integration of graphene in transistors on the scale of 2nm and below addresses known technical and cost barriers to using standard copper integration techniques, where expensive lithography and process “tricks” are necessary to deliver functional devices.

Using graphene in larger scale devices, i.e. resolutions >5nm, is likely to occur, but at a slower pace as the incorporation of graphene interconnects will undoubtedly be more and more of a cost play for the device manufacturers. These cost trade-offs include the changeover cost in equipment, material and process flows.

In other words, for larger scale devices, the decision to incorporate graphene as an interconnect material will be all about cost-effective adoption into already qualified and (presumably) profitable device production lines.

Fabless chip companies need graphene interconnects as well

Fabless chip companies, such as NVIDIA, AMD, Broadcom etc, design their own chips, but outsource the actual production to specialists, such as TSMC, UMC, DB Hitek etc. We also consider Apple and Google to be fabless chip companies given they largely design their own chips for their specific applications. In Apple’s case it designs some of the chips used in its iPhones,

MacBooks, the Apple Watch etc in-house, while Google designed the Tensor G4 for the Pixel 9 and the Tensor Processing Unit (TPU) for neural network machine learning using its proprietary TensorFlow software.

Chip companies don't like to see performance gains of very small resolution chips be undone by the limitations of copper interconnects.

Even though these fabless chip companies don't manufacture chips themselves, they will be very interested in anything that improves the performance of their leading-edge chip designs, i.e. they won't like to see part of the performance gains of their most advanced chips be undone by the limitations of copper interconnects.

2D Generation can apply various commercialisation models

Even though 2D Generation is still a few years away from commercialisation, we need to look at the various revenue models that the company can apply once it has delivered Proof-of-Concept.

The most obvious model would be to license out its IP to anyone who wants to use the technology. For instance, an OEM may want to license the technology and would typically pay a one-off license fee as well as royalties once the manufacturing tool that uses 2D Generation's IP goes into a production line at a chip manufacturer. 2D Generation would likely also receive some non-recurring engineering (NRE) fees to help its customer make custom adjustments to the process if needed.

A similar revenue model could apply in case a chip manufacturer licenses the technology from 2D Generation directly rather than through an OEM.

License fees, royalties and NRE fees.

License fees in the semiconductor industry can range from a few hundred thousand dollars to several million dollars, depending on the uniqueness and potential of the technology. Royalty percentages range from low single digits to the mid-teens, again depending on the technology. Typically, though, they are less than 5% of revenues.

An exclusive license or a takeover?

One of the biggest variables in these revenue models is exclusivity, i.e. whether or not the licensee wants to be the exclusive holder of the IP license so that no other company can use the technology. Exclusive IP licenses are much more expensive than non-exclusive licenses, because the technology can only be licensed out once as opposed to non-exclusive licenses that can be licensed to multiple parties.

An outright takeover would make more sense than an exclusive license.

In that situation, it might make a lot more sense for the licensee to just acquire the IP owner entirely in order to avoid paying royalties for as long as the technology is being used commercially. It also takes away any uncertainty for the licensee regarding a competitor potentially acquiring the licensor and cancelling the license.

> *We believe this may turn out to be a very realistic scenario in the case of 2D Generation, i.e. a semiconductor OEM with a strong presence in ALD that wants to acquire the entire business once Demo Prototype has been delivered.*

In this scenario, the short list of strategic buyers would be very short indeed and would include Applied Materials, Lam Research, ASM International and Tokyo Electron, in our view, given they would have deep enough pockets.

Adisyn's original activities have big potential

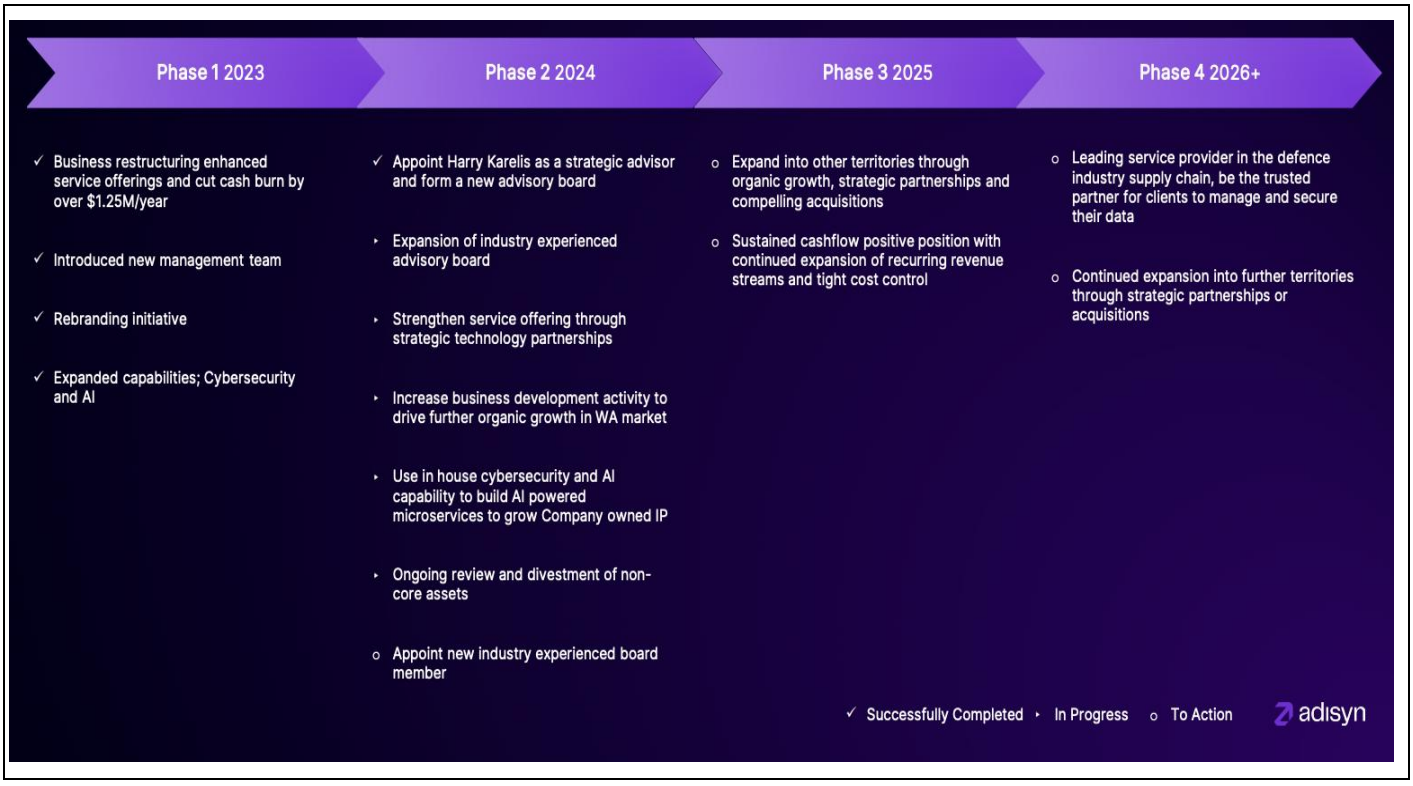
Moving up the value chain.

Adisyn's legacy business provides managed technology services and solutions, aiming to be the preferred sovereign provider for SMEs in the Australian defence industry supply chain. The company has no intention of divesting this business and sees it as complementary to 2D Generation.

Adisyn was founded in 2012 as DCTwo and focused on providing cloud services delivered from data centres in Perth and Darwin. The company is currently in the middle of a strategic adjustment that began in 2023 when it changed its name from DCTwo to Adisyn, shifted its focus to generative AI solutions and microservices, and brought in new management.

During 2024, it has focused on expanding its advisory board and business development activities, while disposing of non-core assets within the business. In the next couple of years, it will be seeking Australia-wide expansion (through both organic growth and acquisitions) as well as expansion in WA (Figure 9).

Figure 9: Adisyn's strategic adjustment timeframe



Source: Company

SMEs need to be able to handle cybersecurity threats and need a trusted specialist partner that can aid with protection from threats, regulatory compliance and IT security infrastructure. Adisyn can help because of its expansive suite of services tailored to individual client needs, including Security Awareness Training, Secure Data Management & Encryption, Identify & Access Management (IAM) and AI Application Enablement.

The Defence industry in WA is a very big market opportunity

It is difficult to measure a figure across Australia, but there is an opportunity of 220 businesses and contractors in WA alone – this is the number of entities that have registered from defence capability with Defence West. Nonetheless, this is still a lucrative opportunity, because a significant proportion of Australia's defence projects and AUKUS-related activities are there.

Of particular note are the Australian Marine Complex in Henderson and the HMAS Stirling Naval base, south of Perth. AUKUS is expected to generate up to 8,500 direct jobs, with an extra 500 jobs for maintenance of submarines (including nuclear-powered submarines) between 2027-2032.

Government-funded Cyber Security spending within the Defence sector is expected to double to $6bn.

Canberra plans to inject an extra $5.7bn into its defence capability by 2027-28, with an extra $50.3bn allocated from then until 2033-34, escalating the budget to $100bn annually by 2033-34 for a total of $765bn.

Of that, $15-20bn will be specifically earmarked to bolster cyber domain capabilities during this period. The state government is injecting into the industry too, targeting a doubling of its size to $6bn by 2030.

Our Valuation of Adisyn: A Sum-of-the-Parts

We have valued Adisyn using a Sum-of-the-Parts methodology.

We have valued Adisyn using a Sum-of-the-Parts (SOTP) valuation. We believe this methodology is appropriate in this instance for several reasons.

Firstly, Adisyn's existing services business, although not profitable yet, has been generating revenues for many years. In FY24, apart from one-off gains and non-operating income, it generated $5.5m in revenues. This makes this business easy to model in a Discounted Cashflow (DCF) model. By contrast, 2D Generation is still in the development phase of its technology and is still several years away from initial revenues. We have therefore turned to peer group valuations and Mergers & Acquisitions (M&A) activity in the semiconductor sector to get a sense of value for this business.

Secondly, both activities have quite different peer groups on ASX, i.e. Cloud Services and Data Centre stocks on the one hand and semiconductor-related stocks on the other. Both have different dynamics and valuations.

Lastly, similar to the (Crypto) Miner Hosting division that is currently being sold, we believe there is a possibility Adisyn could divest its existing data centre business in due course. So, it makes sense to look at the valuation of the individual businesses standalone, in our view.

Valuing 2D Generation

In order to put a value on 2D Generation in a standalone scenario, we have made an ASX peer group valuation comparison. Additionally, we have looked at M&A transactions in the semiconductor space in recent years given that semiconductor equipment OEMs, such as Lam Research, ASM International and Applied Materials, have been quite acquisitive in the space over the last few decades.

Peer group valuation shows Adisyn is substantially undervalued

Starting with our peer group valuation (Figure 10), we have included very specific semiconductor IP development companies listed on ASX that are at varying stages of development. Some, like Weebit Nano (ASX:WBT) and BrainChip (ASX:BRN), are in the process of commercialising and have already received initial license fee income. Others, like 4DS Memory (ASX:4DS) and Nanoveu (ASX:NVU) are still very much in the development stage.

Figure 10: Peer group valuation

Company	Ticker	shares (m)	Share Price (A$)	Market Cap (A$ m)
4DS Memory	4DS	1,763.4	0.044	77.6
Archer Materials	AXE	254.8	0.37	93.0
AudioPixels	AKP	29.2	6.20	181.0
BluGlass	BLG	1,839.3	0.025	46.0
BrainChip	BRN	1,972.5	0.33	646.0
Nanoveu	NVU	542.7	0.034	18.5
Weebit Nano	WBT	206.6	2.62	541.3
Average				***229.1***
Average valuation of AXE and AKP				***137.0***
Adisyn	**AI1**	**617.3**	**0.07**	**43.2**

Source: Company

AudioPixels (ASX:AKP) and Archer Materials (ASX:AXE) are the best comparables for 2D Generation, in our view, as they are likely just a few years away from commercialisation.

Relevant ASX-listed sector peers are valued 3.2x higher than Adisyn.

So, when looking at the average valuation of this peer group, which comes in at A$229m, one could argue it is skewed because of the relatively high valuations of WBT and BRN given that these companies are in full commercialisation mode, while a stock like Nanoveu might be dragging the average down too much.

Just 2D Generation is potentially worth $0.22 per share on its own.

For this reason, we have specifically looked at the average valuation of the peer group excluding these "outliers". Put differently, we have used the average valuation of AXE and AKP (trading suspended currently) as a guide to AI1's valuation. This average comes in at A$137m, or A$0.22 per share, which is ~3.2x Adisyn's current market capitalisation!

So, while Adisyn last traded at $0.07 per share, we believe 2D Generation is potentially worth $0.22 per share just standalone.

Very attractive risk/reward proposition.

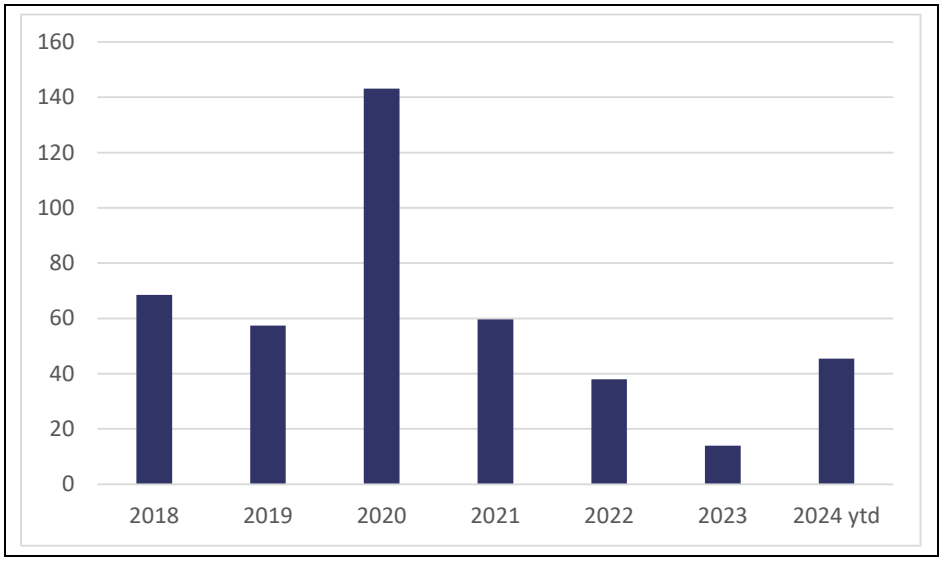
Both AXE and AKP have been working on the development of their respective technologies a lot longer than 2D Generation and have invested substantially more funds in that development. At the same time, we believe there is a very high probability that 2D Generation will be able to commercialise before both AKP and AXE. In other words, we believe 2D Generation provides investors with a highly attractive risk/reward proposition.

Too early to talk about valuation in M&A scenario

The semiconductor industry has been very acquisitive in the last few decades.

The semiconductor industry has always been very open to Mergers & Acquisitions as illustrated by Figure 11. And these takeovers have not only been focussed on large, established companies. The industry is always specifically looking to acquire semiconductor IP as well, in manufacturing, equipment and software. And as the data shows, the value of the acquisitions over time is just as cyclical as the semiconductor industry itself.

Figure 11: Value of semiconductor M&A deals (US$ bn)



Source: KPMG, MergerMarket

When it comes to semiconductor equipment M&A specifically, we have found a number of acquisitions done by some of the larger semiconductor

equipment OEM's in the last few years (Figure 12) adjacent to the area 2D Generation is active in.

Figure 12: Value of semiconductor M&A deals (US$ m)

Target	Acquirer	Acquired technology	Year	Valuation US$
Epiluvac	Veeco	CPV for SiC wafers	2023	56
Entrepix	Amtech systems	Chemical Mechanical Polishing	2023	39
Semsysco	Lam Research	Electrochemical deposition	2022	n.a.
LPE	ASM International	Epitaxial reactors	2022	450
Picosun	Applied Materials	Atomic Layer Deposition	2022	n.a.
HPSP	Hanmi	Hydrogen annealing	2021	223
Average valuation				***192***

Source: Pitt Street Research, Arthos Corporate Finance

As is clear from the data, or lack thereof, it is very hard to derive a potential takeover valuation for 2D Generation once it delivers Proof-of-Concept. Even though the valuation numbers are clearly higher than Adisyn's current valuation, they vary widely and the value of some deals hasn't been disclosed.

On top of that, 2022 and 2023 weren't the best years to sell a company given the semiconductor bear market in 2022 and the, only modest, upcycle in 2023.

Valuation in a potential takeover scenario will very much depend on market sentiment and buyer urgency.

In other words, when it comes to valuing 2D Generation in a takeover scenario, we don't attribute too much value to this past data. If and when the company becomes a takeover target, we believe the value will depend on the market sentiment at that time and how badly the acquirer wants to own 2D Generation's IP.

Suffice it to say, we believe a potential acquirer of 2D Generation will most likely be a semiconductor equipment OEM, like Applied Materials, Lam Research, Tokyo Electron or ASM International, given that these companies should be able to derive more value from such a deal than semiconductor manufacturers or fabless companies, in our view.

Valuing Adisyn's existing Services business

We value Adisyn's existing data business at $43.7m or $0.071 per share in our base case and $61.6m or $0.10 per share in our bull case (Figure 13).

Figure 13: DCF valuation of Adisyn's existing services business

Valuation (A$m)	Base Case	Bull case
Present Value of FCF	21.9	29.1
Present Value of Terminal Value	22.4	33.0
Enterprise Value (A$ m)	**44.3**	**62.2**
Net (debt) cash	(0.6)	(0.6)
Equity value (A$ m)	**43.7**	**61.6**
Shares outstanding	617.3	617.3
Implied price (A$ cents)	**0.071**	**0.10**

Estimates: Pitt Street Research

We acknowledge these are discounts to the current share price, but are premiums to the 30-Day VWAP prior to the acquisition[4], which was $0.037 per share. We have used a DCF (Discounted Cash Flow) methodology, using 10-years of forecasted cash flows and 2% terminal growth thereafter.

- **Revenue growth**: Observing Adisyn's individual units, we assume the data centre and cloud services gradually winds down over the next two years, but its managed support services and project revenue grows by 90% in FY25, 65% in FY26, 40% in FY27 and gradually moderating to 5% by FY34. This may appear optimistic, but is more conservative than the 618% and 256% increases in managed support services and project revenues respectively. Our bull case assumes 100% in FY25, then 70% in FY26, 50% in FY27 and moderating growth thereafter. By FY34, our base case model assumes $47m in revenue, whilst our bull case suggests $62m in revenue.
- **Expenses**: We model most expenses as a percentage of revenue similar to the current proportions: Cost of sales 40%, selling and distribution 2%, with a further 40% provisioned for other operating expenses. The exception is administrative expenses where we model 5% cost inflation annually. The result will see Adisyn record its first profit in FY26, at a narrow 2% margin, and margins growing to 18% by FY29 and staying there for the rest of the life of our model. Our bull case has similar assumptions and ends up with a 19% profit margin by the end of the life of our model, although we assume the first profit in FY25 with a 1% profit margin, followed by a 5% margin In FY26.
- **Tax**. We model 25% corporate tax in light with the rate for Australian companies with revenue below $50m. Even in our bull case, the company does not exceed this.
- **Discount rate**. We model 13.1% based on a 1.5x beta, a 4.7% risk-free rate of return and an 6% equity premium.
-

Investors are getting the upside from 2D Generation for free

At the current share price, investors are getting the upside from 2D Generation for free.

We acknowledge that the share price derived from our equity value for Adisyn's existing business is not significantly higher than the current share price. However, it is worth noting that the shares have significantly re-rated since its announcement of the acquisition of 2D Generation on 4 November.

> *Another way to look at this valuation is that it basically tells us that, at the current Adisyn share price, investors are buying the existing business and are getting the upside from 2D Generation for free!*

Conclusion: Valuation of A$0.29 per share

As discussed previously, we believe Adisyn's two businesses are very distinct and can be operated as such. This also means they can be individually divested if and when that becomes opportune, hence our Sum-of-the-Parts approach to valuing Adisyn. Combining our valuation for 2D Generation of A$0.22 with the approximate A$0.07 valuation for Adisyn's existing services business in our base case, we arrive at a Sum-of-the-Parts valuation of A$0.29 per share on a 12-month investment horizon.

[4] 30 trading days prior to 4 November 2024

Potential share price catalysts

We see the following share price catalysts:

- We expect 2D Generation will have regular news flow around its graphene deposition development work in the near to medium term.
- Positive progress reports around the company's work with imec and the ConnectingChips collaboration.
- Possible announcements of additional semiconductor industry collaborations in the near to medium term.
- Delivery of Demo Prototype of graphene interconnects using ALD, expected in 2026.
- The services business becoming profitable within the next 18 months.
- Potential takeover/divestment of either Adisyn's existing data centre business and/or 2D Generation in due course.

Risks

We see the following key risks to our investment thesis:

- **Funding risk**: Adisyn/2D Generation will require significant funding to realise its development and commercial ambitions. An inability to secure financing on favourable terms, or failure to secure funding at all, could be catastrophic for the company.
- **Technology risk**: There is the risk that the company may not move fast enough to keep pace with the competition. Additionally, in case 2D Generation's patents are infringed, there is no guarantee that the company can defends these patents in court given the substantial financial burden this would involve.
- **Cyber/Infrastructure risk**: A failure or interruption of the company's cyber systems or infrastructure systems could cause significant problems for the company's development program.
- **Commercial risk**. There is the risk that the company may fail to execute its commercial objectives for a variety of reasons including competition and lack of acceptance by the market.
- **Key personnel risk**: There is the risk the company may lose key personnel and may be unable to replace them and/or their contribution to the business

Appendix I: Board and Management Team

Board of Directors & Management	
Name and Designation	**Profile**
Shane Wee Non-Executive Chairman	Mr. Wee is a highly experienced professional in the financial services sector, bringing a wealth of expertise to the board. With over three decades of experience and a strong background in ASX, he played a crucial role as a Founding Director of Alto Capital, holding various corporate and advisory positions within multiple ASX entities. Throughout his successful career, Mr Wee has built an extensive network of contacts across Australia and South-East Asia.
Blake Burton Managing Director	Mr. Burton has been serving as the Managing Director of Adisyn since July 2022. Prior to joining Adisyn, he founded and successfully sold his web hosting company to Australia's largest privately owned web host. With a background in auditing for ASX-listed and international companies, Mr Burton has also held directorial roles in various companies. He is a graduate of the University of Western Australia, holding a Bachelor of Commerce with a specialisation in Accounting and Corporate Finance.
Justin Thomas Non-Executive Director (Expected to step down at appointment of Arye Kohavi)	Mr Thomas has over 20 years of experience in the IT Industry, he has made remarkable accomplishments throughout his career. In 2007, he successfully established and eventually sold a real estate software business. In 2012, Mr Thomas ventured into the data centre industry, where he designed and sold his first Data Centre to Amcom, which is now known as Vocus. Today, he leverages his expertise in the IT industry to explore new technologies and develop innovative solutions for businesses of all sizes. He will stand down as director upon the appointment of Arye Kohavi.
Arye Kohavi Non-Executive Director/CEO of 2D Generation (Expected to be appointed as Non-Executive Director on receipt Director Identification Number)	Mr Kohavi will join the board subject to shareholder approval at the meeting to make the acquisition of 2D Generation official. 2D is entitled to appoint one nominee to the board and Mr Kohavi is the nominee. Mr Kohavi is an Israeli entrepreneur and innovator. He was the founder, president and co-CEO of Water-Gen, which develops water-from-air and air dehumidification technologies. Mr Kohavi holds an MBA (Finance) and a BA in Economics and Accounting, both from the Hebrew University in Jerusalem. He has won a number of awards as part of his time at Water-Gen including being chosen as one of the world's top 100 Leading Global Thinkers, and one of the world's top innovators by *Foreign Policy* magazine; and Water-Gen has won awards including being chosen as one of the 'Nine Greatest Israeli Inventions of All Times' from the Israeli Ministry of the Economy, and being one of the world's best 100 inventions of the year in 2019 by TIME magazine.
Itzhak Edrei Co-founder of M&T Semiconductor	Dr Edrei is a longstanding business leader in the semiconductor industry, having held several high-level roles at Tower Semiconductor including President, and is currently serving as Tower's President Emeritus. Dr Edrei established Tower's R&D and Business Units divisions, playing a key role in growing organic and inorganic revenue from $100m to $1.3bn. This included setting up multiple key business units, signing long-term agreements with customers, and then identifying and executing on M&A opportunities.

Zmira Shterenfeld-Lavie Co-founder of M&T	Ms Shterenfeld-Lavie has led diverse projects and processes within the semiconductor industry for more than 30 years, amassing significant R&D process development expertise, including technology development and transfers (CMOS, sensors, MEMs, discrete etc.). As general manager of Tower Semiconductor's TOPS (Transfer Optimisation and development Process Services) business unit, she took the business unit's annual revenue from zero to US$200m.
Miri Kish Dagan VP of R&D	Ms Kish-Dagan was the VP R&D and the CTO of Raicol crystals that specializes in the manufacture of high-quality nonlinear optical crystals and electro-optic devices. She was leading development from inception to prototype in the semiconductors , medical, military, and space application. She has over 19 years of experience with engineering processing, technologies and R&D management in fabrication and tool installation. Prior to Raicol, she served at Suron as VP of R&D engineering, and in various positions at Tower semiconductors. She received her MSc and BSc in Material Engineering from Ben-Gurion University in Israel. Winner of the *Pioneering Women Award* for *groundbreaking* achievements in the high-tech sector given to her by the Israeli Hi-Tech Association and the Manufacturers Association of Israel.
Paul Rich Technology Leader	Mr Rich has more than 35 years of experience in the semiconductor industry. Paul was the Vice President for Technology and Engineering at SPTS Technologies, where he managed the product development team until December 2022. SPTS develops and manufactures advanced wafer processing solutions for the world's leading semiconductor and microelectronic device manufacturers. Mr. Rich graduated from Bath University in 1987 with a B.Sc in Physics. He has published numerous technical articles and has several patents relating to plasma processing.

Source: Company

Appendix II – Capital Structure

Class	Number	%
Ordinary Shares	617,287,439	62.1%
Performance rights	309,000,000	31.1%
Options	68,000,000	6.8%
Diluted shares	**994,287,439**	

Source: Company

Appendix III – Patents

File Reference	Applicant	Application No.	Pub. No.	App Date	Title	Status
14801-US1	2D Generation Ltd Bar Ilan University (Ref. 7738-US)	18/574,061	US2024/0301554A1	29/6/2022	GRAPHENE COATED NON-METALLIC SURFACES, DEVICES AND METHOD THEREOF	Pending
14801-PC	2D Generation Ltd Bar Ilan University (Ref. 7738-WO)	PCT/IL2022/050701	WO2023/275873A1	29/6/2022	GRAPHENE COATED NON-METALLIC SURFACES, DEVICES AND METHOD THEREOF	National Phase
14802-US1	2D Genereation Ltd Bar Ilan University	18/692,223	N/A	20/9/2022	GRAPHENE COATED METALLIC SURFACES, DEVICES AND METHOD OF MANUFACTURE THEREOF	Pending
14802-PC	2D Genereation Ltd Bar Ilan University (Ref. 7744-WO)	PCT/IL2022/051010	WO2023/042210A1	20/9/2022	GRAPHENE COATED METALLIC SURFACES, DEVICES AND METHOD OF MANUFACTURE THEREOF	National Phase
14803-EP1	2D Genereation Ltd Bar Ilan University - 7754-PCT-EP	23708916.4	N/A	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14803-IL1	2D Genereation Ltd Bar Ilan University - 7754-PCT-EP	314976	314976	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14803-US1	2D Genereation Ltd Bar Ilan University - 7754-PCT-US	18/835,836	N/A	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14803-PC	2D Genereation Ltd Bar Ilan University - 7754-WO	PCT/IL2023/050158	WO2023156997A1	15/2/2023	METHOD OF MANUFACTURE OF GRAPHENE COATED SURFACES BY ATOMIC OR MOLECULAR LAYER DEPOSITION	Pending
14804-USP2	2D Genereation Ltd Bar Ilan University	63/690,518	N/A	4/9/2024	Graphene-Metal Complex	Pending

Source: 2D Generation

Appendix IV – Top 20 Shareholders

	Group/Holder Name	Holding	%
1	IBI CAPITAL COMPENSATION ANDTRUSTS (2004) LTD<ORI ACKERMAN>	37,362,559	6.05
2	IBI CAPITAL COMPENSATION ANDTRUSTS (2004) LTD<KOBI BEN-SHABATH>	37,362,558	6.05
3	SENVEST TECHNOLOGY PARTNERSMASTER FUND LP	24,660,701	4.00
4	IBI TRUST MANAGEMENT<PROF DORON NAVEH>	21,479,702	3.48
5	BURTON CAPITAL HOLDINGS PTY LTD <BURTON INVESTMENT A/C>	16,416,028	2.66
6	IBI CAPITAL COMPENSATION ANDTRUSTS (2004) LTD<ARYE KOHAVI>	15,300,846	2.48
7	THOMAS FAMILY HOLDINGS PTY LTD	14,578,396	2.36
8	BNP PARIBAS NOMSPTY LTD	13,693,288	2.22
9	SANDTON CAPITAL PTY LTD<SANDTON FAMILY A/C>	12,790,666	2.07
10	IBI TRUST MANAGEMENT<BIRAD R& D COMPANY LTD A/C>	11,606,432	1.88
11	TRINDIS PTY LTD	11,000,000	1.78
12	IBI TRUST MANAGEMENT<MENNI MOR>	9,816,596	1.59
13	LIBERTINE INVESTMENTS PTY LTD	8,464,518	1.37
14	IBI TRUST MANAGEMENT<ODED MOR>	8,413,707	1.36
15	MR SHANE HOEHOCK WEE<WEE FAMILY A/C>	8,387,703	1.36
16	SENVEST GLOBAL (KY) LP	8,220,234	1.33
17	FINCLEAR SERVICES PTY LTD<SUPERHERO SECURITIES A/C>	7,942,607	1.29
18	IBI TRUST MANAGEMENT<SHIMON ERLICHMAN>	7,318,755	1.19
19	GEMELLI NOMINEES PTY LTD<GEMELLI FAMILY A/C>	6,850,000	1.11
20	SUPAVAL PTY LTD<SUPAVAL SUPER FUND A/C>	6,064,335	0.98

Appendix V – Analysts' Qualifications

Marc Kennis has been an equities analyst since 1996.

- Marc obtained an MSc in Economics from Tilburg University, Netherlands, in 1996 and a postgraduate degree in investment analysis in 2001.
- Since 1996, he has worked for various brokers and banks in the Netherlands, including ING and Rabobank, where his focus has been on the technology sector, including the semiconductor sector.
- After moving to Sydney in 2014, he worked for several Sydney-based brokers before setting up TMT Analytics Pty Ltd, an issuer-sponsored equity research firm.
- In July 2016, with Stuart Roberts, Marc co-founded Pitt Street Research Pty Ltd, which provides issuer-sponsored research on ASX-listed companies across the entire market, including technology companies.

Nick Sundich is an equities research analyst at Pitt Street Research.

- Nick obtained a Bachelor of Commerce/Bachelor of Arts from the University of Sydney in 2018. He has also completed the CFA Investment Foundations program.
- He joined Pitt Street Research in January 2022. Previously he worked for over three years as a financial journalist at StockHead.
- While at university, he worked for a handful of corporate advisory firms.

General advice warning, Disclaimer & Disclosures

Terms & Conditions

The information contained herein ("Content") has been prepared and issued by Pitt Street Research Pty Ltd ACN 626365615 ("Pitt Street Research"), an Authorised Representative (no: 1265112) of BR Securities Australia Pty Ltd. ABN 92 168 734 530, AFSL 456663. All intellectual property relating to the Content vests with Pitt Street Research unless otherwise noted.

Disclaimer

Pitt Street Research provides this financial advice as an honest and reasonable opinion held at a point in time about an investment's risk profile and merit and the information is provided by the Pitt Street Research in good faith. The views of the adviser(s) do not necessarily reflect the views of the AFS Licensee. Pitt Street Research has no obligation to update the opinion unless Pitt Street Research is currently contracted to provide such an updated opinion. Pitt Street Research does not warrant the accuracy of any information it sources from others. All statements as to future matters are not guaranteed to be accurate and any statements as to past performance do not represent future performance.

Assessment of risk can be subjective. Portfolios of equity investments need to be well diversified and the risk appropriate for the investor. Equity investments in a listed or unlisted company yet to achieve a profit or with an equity value less than $50 million should collectively be a small component of an individual investor's equity portfolio, with smaller individual investment sizes than otherwise. Investors are responsible for their own investment decisions, unless a contract stipulates otherwise.

Pitt Street Research does not stand behind the capital value or performance of any investment. Subject to any terms implied by law and which cannot be excluded, Pitt Street Research shall not be liable for any errors, omissions, defects or misrepresentations in the information (including by reasons of negligence, negligent misstatement or otherwise) or for any loss or damage (whether direct or indirect) suffered by persons who use or rely on the information. If any law prohibits the exclusion of such liability, Pitt Street Research limits its liability to the re-supply of the Information, provided that such limitation is permitted by law and is fair and reasonable.

General advice warning

The Content is General Financial Advice but has been prepared for general information purposes only and is not (and cannot be construed or relied upon as) Personal Financial Advice nor as an offer to buy/sell/subscribe to any of the financial products mentioned herein. No investment objectives, financial circumstances or needs of any individual have been taken into consideration in the preparation of the Content.

Financial products are complex, entail risk of loss, may rise and fall, and are impacted by a range of market and economic factors, and you should always obtain professional advice to ensure trading or investing in such products is suitable for your circumstances, and ensure you obtain, read and understand any applicable offer document.

Disclosures

Pitt Street Research has been commissioned to prepare the Content. From time to time, Pitt Street Research representatives or associates may hold interests, transact or hold directorships in, or perform paid services for, companies mentioned herein. Pitt Street Research and its associates, officers, directors and employees, may, from time to time hold securities in the companies referred to herein and may trade in those securities as principal, and in a manner which may be contrary to recommendations mentioned in this document.

Pitt Street Research receives fees from the company referred to in this document, for research services and other financial services or advice we may provide to that company. The analyst has received assistance from the company in preparing this document. The company has provided the analyst with communication with senior management and information on the company and industry. As part of due diligence, the analyst has independently and critically reviewed the assistance and information provided by the company to form the opinions expressed in the report. Diligent care has been taken by the analyst to maintain an honest and fair objectivity in writing this report and making the recommendation. Where Pitt Street Research has been commissioned to prepare Content and receives fees for its preparation, please note that NO part of the fee, compensation or employee remuneration paid will either directly or indirectly impact the Content provided.